



**Model Name:GA-970A-DS3**

### Component value change history


**Version: 1.0**

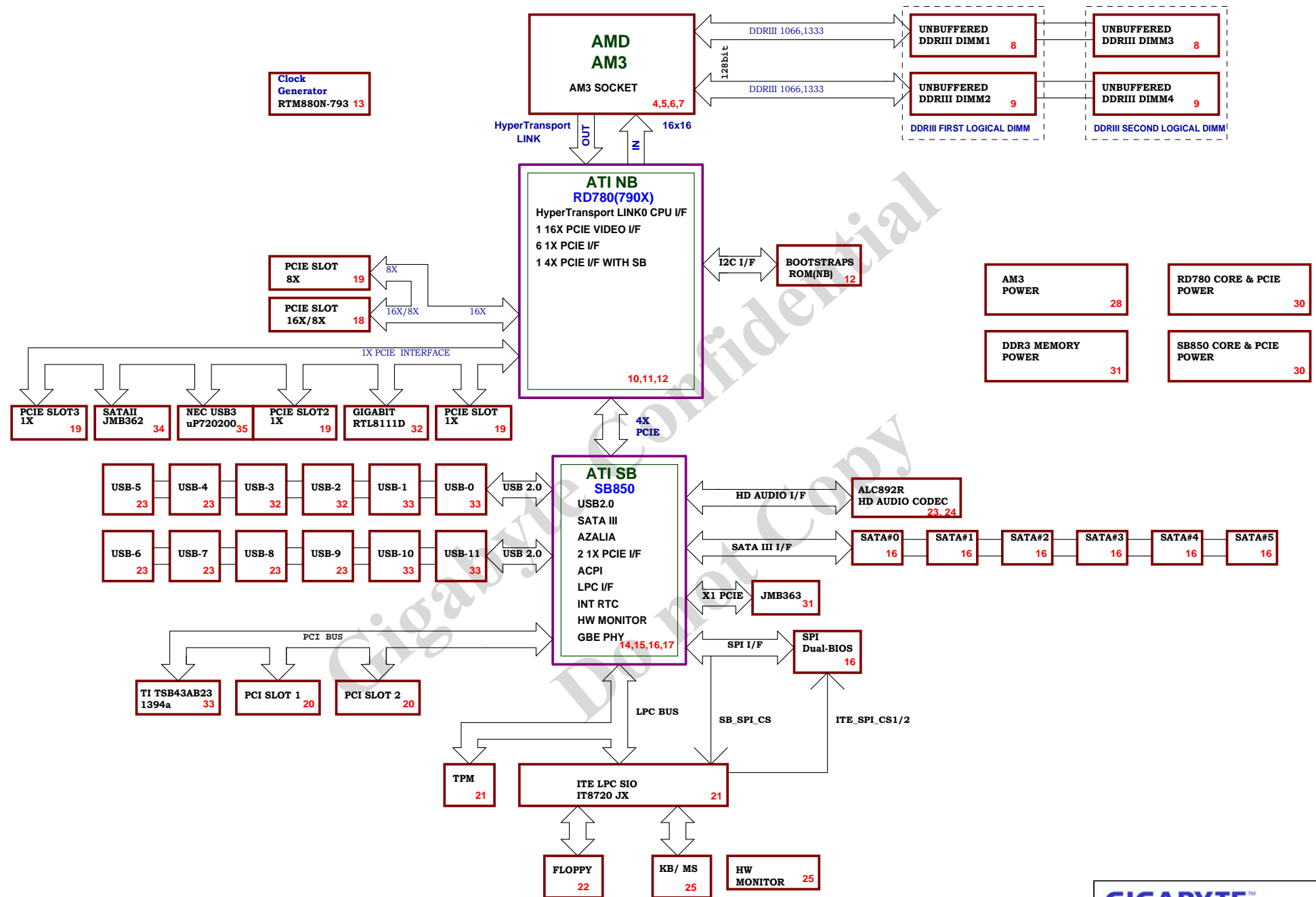
**P-Code: U98094-0**

[illegible]

### Circuit or PCB layout change for next version

[illegible]

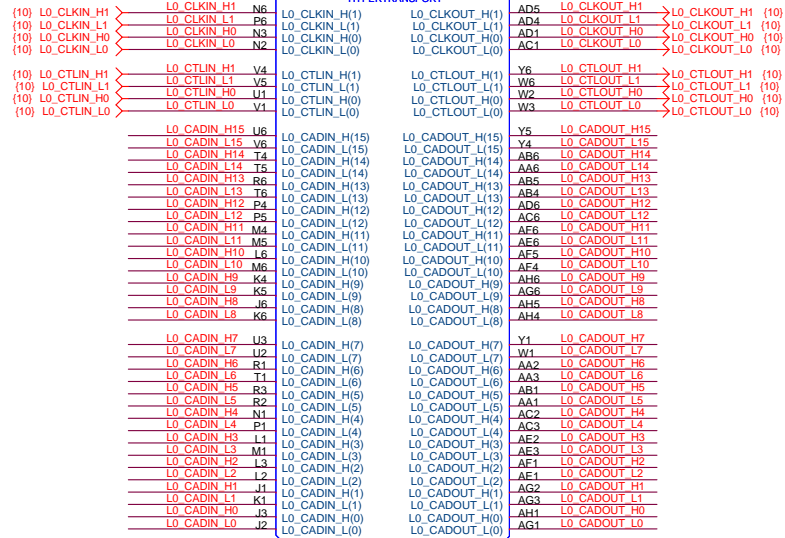
			
Title			
<p align="center"><b>BOM &amp; PCB HISTORY</b></p>			
Size	Document Number	Rev	
Custom	<b>GA-970A-DS3</b>	<b>1.0</b>	
Date:	Tuesday, February 07, 2012	Sheet	2 of 36



L0\_CADIN\_L[0..15] <L0\_CADIN\_L[0..15] (10)  
 L0\_CADIN\_H[0..15] <L0\_CADIN\_H[0..15] (10)  
 L0\_CADOUT\_L[0..15] <L0\_CADOUT\_L[0..15] (10)  
 L0\_CADOUT\_H[0..15] <L0\_CADOUT\_H[0..15] (10)

## M2CPUA

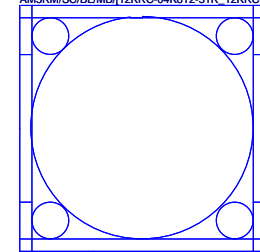
## HYPERTRANSPORT



CPU-SK/942AM3b/S/G/[10SC1-A01942-01R\_10SC1-A01942-02R]

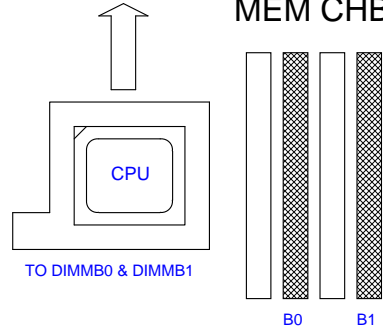
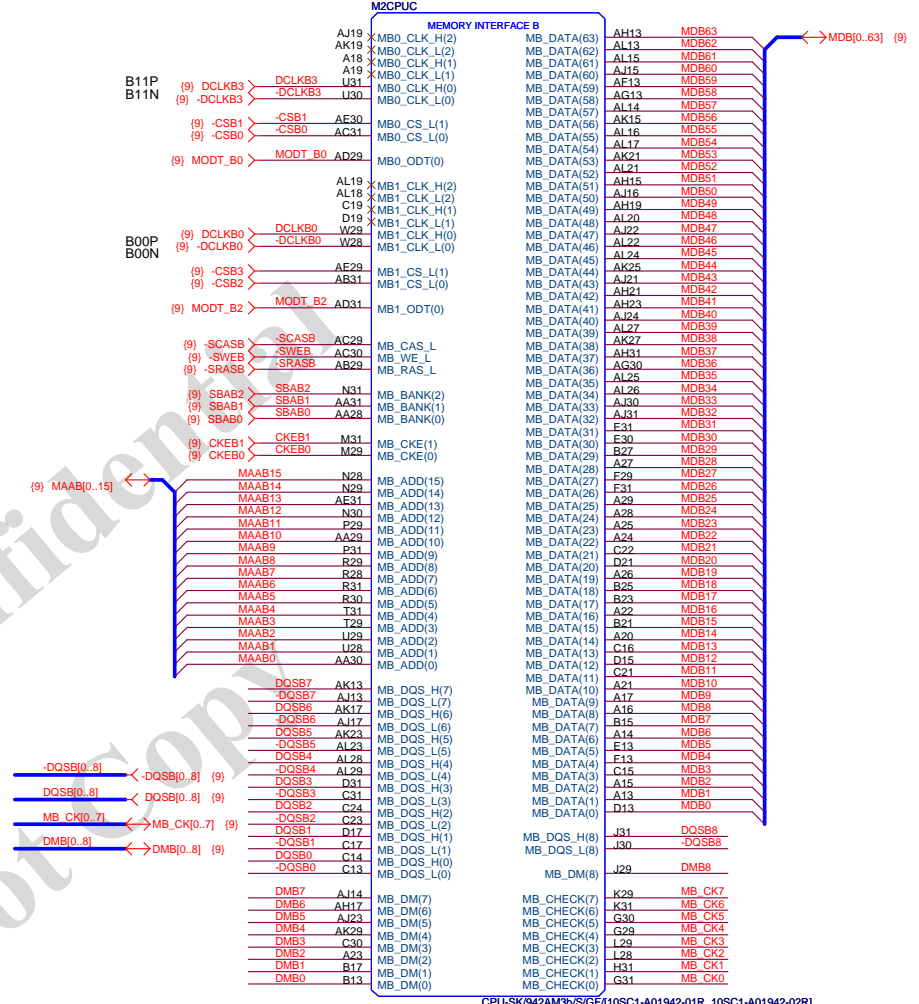
CPU\_VDD\_RUN = VCORE  
 CPU\_VDDA\_RUN = VDDA25  
 VLDT\_RUN = VCC12\_HT  
 CPU\_VDDIO\_SUS = DDR15V  
 CPU\_VDDR = CPU\_VDDR12

VLDT\_A = VCC12\_HT  
 VLDT\_B = HT12B

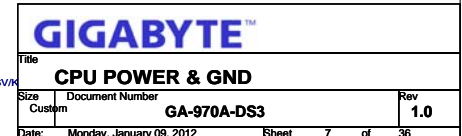
M2CPU  
AM3RM/SC/BL/MB/12KRC-04K812-31R\_12KRC-04K812-32R

GIGABYTE™

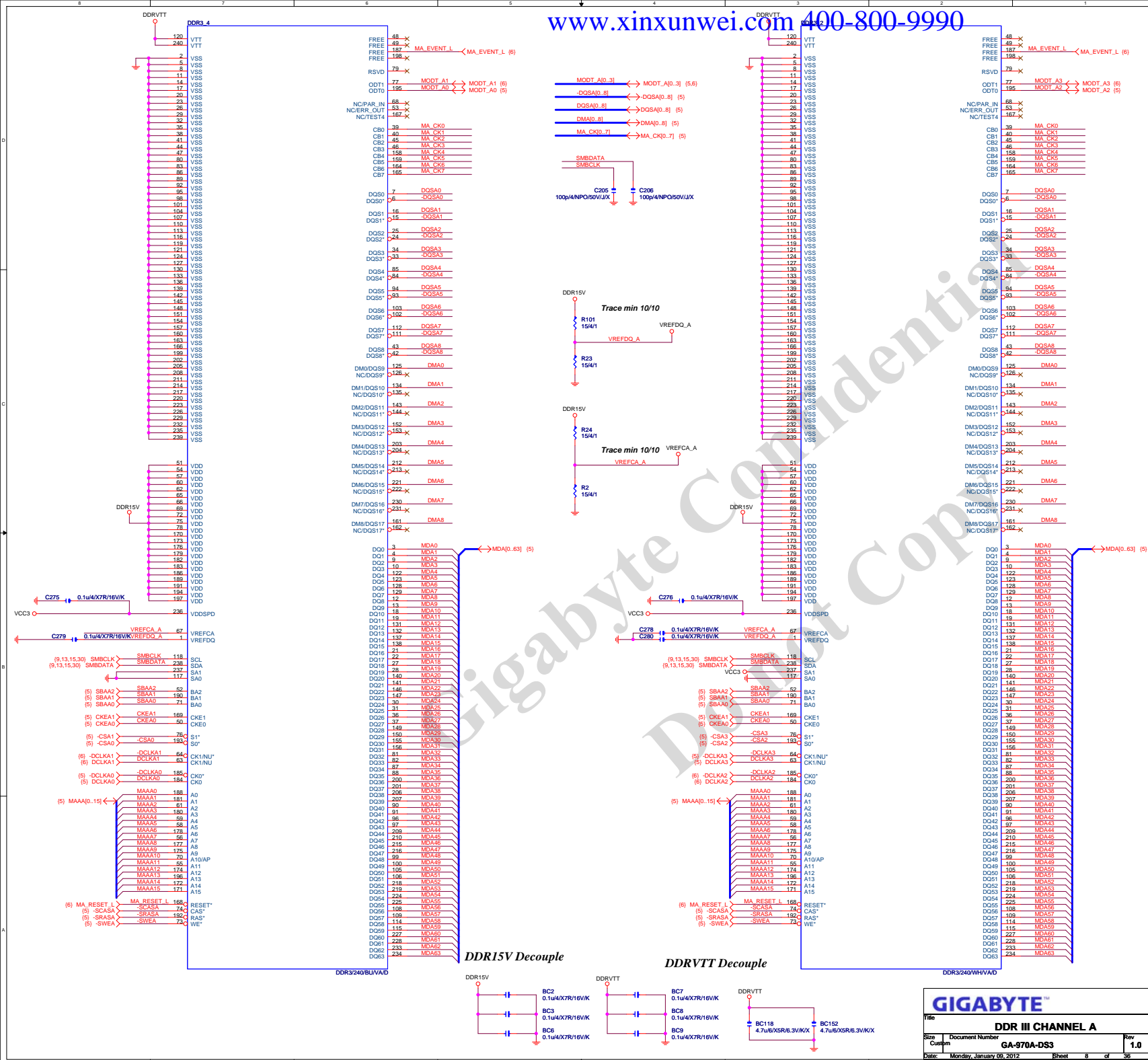
Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-970A-DS3	1.0	
Date:	Monday, January 09, 2012	Sheet	4 of 36



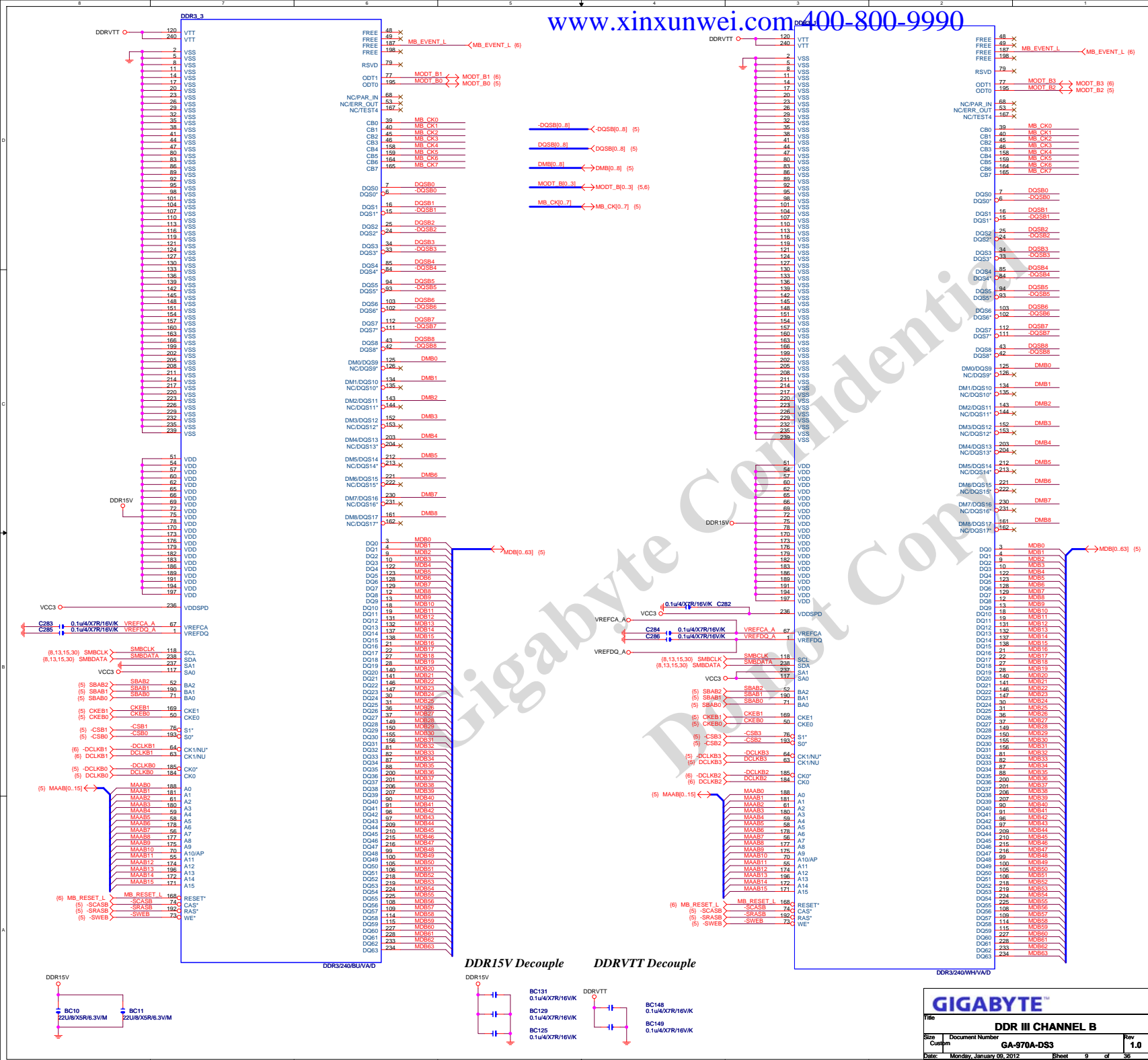


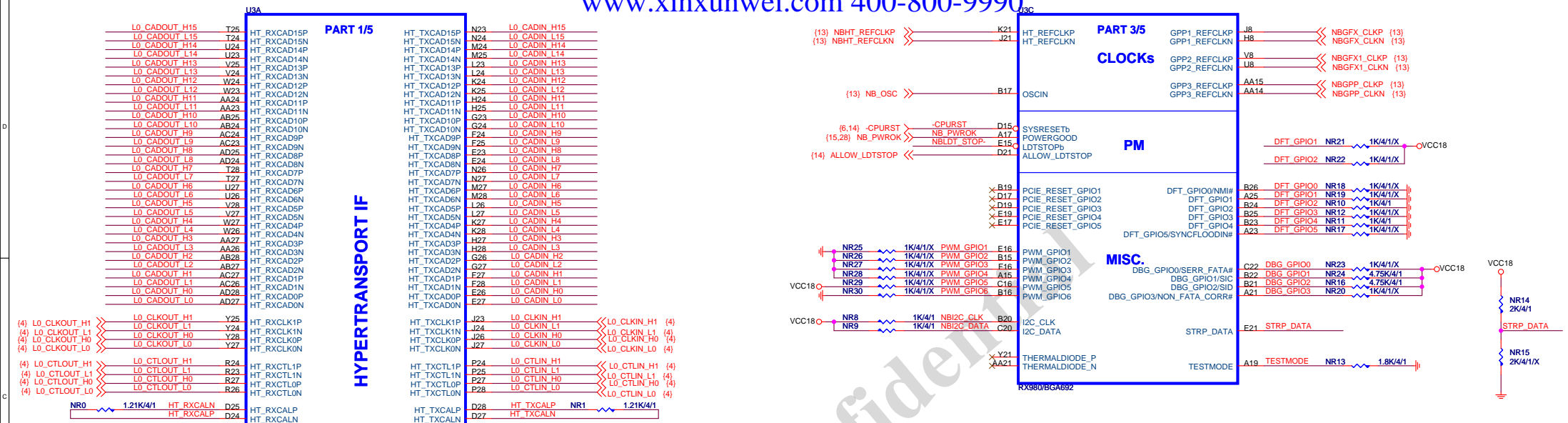












DFT\_GPIO5: STRAP\_DEBUG\_BUS\_GPIO\_ENABLEb

**Enables the Test Debug Bus using GPIO.**  
**1 : Disable ( Can still be enabled using**  
**nbcfg register access)**  
**0 : Enable**

DFT\_GPIO[4:2]: STRAP\_PCIE\_GPP\_CFG[2:0]

**These pin straps are used to configure PCI-E GPP mode.**

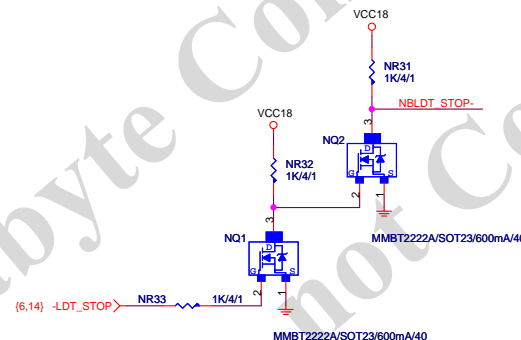
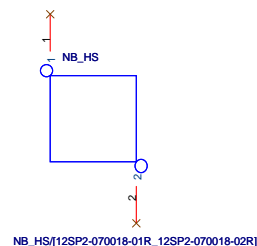
```
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101 : 2:2:2:4 C2
110 : Hardware default (mode L) or EEPROM
111 : Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011
```

## DFT GPIO1: LOAD EEPROM STRAPS

**Selects Loading of STRAPS from EPROM**  
**1** : Bypass the loading of EEPROM straps and use Hardware Default Values  
**0** : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

DFT\_GPIO0: STRAP\_DEBUG\_BUS\_PCIE\_ENABLEb

**Enables the Test Debug Bus using PCIE bus**  
**1 : Disable ( Can still be enabled using nbcfg register access )**  
**0 : Enable**





U3B

PART 2/5

EXP A\_RXP15 N6  
EXP A\_RXN15 N5  
EXP A\_RXP14 M4  
EXP A\_RXN14 M4  
EXP A\_RXP13 L6  
EXP A\_RXN13 L5  
EXP A\_RXP12 K5  
EXP A\_RXN12 K4  
EXP A\_RXP11 J6  
EXP A\_RXN11 J5  
EXP A\_RXP10 H4  
EXP A\_RXN10 H4  
EXP A\_RXP9 G6  
EXP A\_RXN9 G5  
EXP A\_RXP8 F5  
EXP A\_RXN8 F4  
EXP A\_RXP7 D2  
EXP A\_RXN7 D1  
EXP A\_RXP6 B5  
EXP A\_RXN6 C6  
EXP A\_RXP5 D6  
EXP A\_RXN5 E6  
EXP A\_RXP4 E7  
EXP A\_RXN4 F7  
EXP A\_RXP3 D8  
EXP A\_RXN3 E8  
EXP A\_RXP2 F9  
EXP A\_RXN2 F9  
EXP A\_RXP1 D10  
EXP A\_RXN1 E10  
EXP A\_RXP0 E11  
EXP A\_RXN0 F11

PCIE GPP1

GPP1\_RX15P  
GPP1\_RX15N  
GPP1\_RX14P  
GPP1\_RX14N  
GPP1\_RX13P  
GPP1\_RX13N  
GPP1\_RX12P  
GPP1\_RX12N  
GPP1\_RX11P  
GPP1\_RX11N  
GPP1\_RX10P  
GPP1\_RX10N  
GPP1\_RX9P  
GPP1\_RX9N  
GPP1\_RX8P  
GPP1\_RX8N  
GPP1\_RX7P  
GPP1\_RX7N  
GPP1\_RX6P  
GPP1\_RX6N  
GPP1\_RX5P  
GPP1\_RX5N  
GPP1\_RX4P  
GPP1\_RX4N  
GPP1\_RX3P  
GPP1\_RX3N  
GPP1\_RX2P  
GPP1\_RX2N  
GPP1\_RX1P  
GPP1\_RX1N  
GPP1\_RX0P  
GPP1\_RX0N

N3 EXP A\_TXP15  
M2 EXP A\_TXN15  
M1 EXP A\_TXN14  
L3 EXP A\_TXP13  
L2 EXP A\_TXN13  
K2 EXP A\_TXP12  
K1 EXP A\_TXN12  
J3 EXP A\_TXP11  
J2 EXP A\_TXN11  
H2 EXP A\_TXP10  
H1 EXP A\_TXN10  
G3 EXP A\_TXP9  
G2 EXP A\_TXN9  
F2 EXP A\_TXP8  
F1 EXP A\_TXN8  
E3 EXP A\_TXP7  
E2 EXP A\_TXN7  
A4 EXP A\_TXP6  
B4 EXP A\_TXN6  
A6 EXP A\_TXP5  
B6 EXP A\_TXN5  
B7 EXP A\_TXP4  
C7 EXP A\_TXN4  
A8 EXP A\_TXP3  
B8 EXP A\_TXN3  
B9 EXP A\_TXP2  
C9 EXP A\_TXN2  
A10 EXP A\_TXP1  
B10 EXP A\_TXN1  
B11 EXP A\_TXP0  
C11 EXP A\_TXN0

AD9  
AD8  
AE8  
AC7  
AD7  
AD6  
AE6  
AF5  
AG5  
AF2  
AD1  
AD2  
AB5  
AA6  
AA5  
Y5  
Y4  
W6  
W5  
V5  
V4  
U6  
U5  
T5  
T4  
R6  
R5  
P5  
P4

PCIE GPP2

GPP2\_RX15P  
GPP2\_RX15N  
GPP2\_RX14P  
GPP2\_RX14N  
GPP2\_RX13P  
GPP2\_RX13N  
GPP2\_RX12P  
GPP2\_RX12N  
GPP2\_RX11P  
GPP2\_RX11N  
GPP2\_RX10P  
GPP2\_RX10N  
GPP2\_RX9P  
GPP2\_RX9N  
GPP2\_RX8P  
GPP2\_RX8N  
GPP2\_RX7P  
GPP2\_RX7N  
GPP2\_RX6P  
GPP2\_RX6N  
GPP2\_RX5P  
GPP2\_RX5N  
GPP2\_RX4P  
GPP2\_RX4N  
GPP2\_RX3P  
GPP2\_RX3N  
GPP2\_RX2P  
GPP2\_RX2N  
GPP2\_RX1P  
GPP2\_RX1N  
GPP2\_RX0P  
GPP2\_RX0N

AF9  
AG9  
AG8  
AH8  
AF7  
AG7  
AG6  
AH6  
AG4  
AH4  
AE3  
AE2  
AC3  
AC2  
AB2  
AB1  
AA3  
AA2  
Y2  
Y1  
W3  
W2  
V3  
V2  
U3  
U2  
T2  
T1  
R3  
R2  
P2  
P1

AD11  
AC11  
AE12  
AD12  
AD13  
AC13  
AE14  
AD14  
AD15  
AC15  
AE16  
AD16  
AD17  
AC17  
AE18  
AD18  
AD19  
AC19  
AH20  
AG20

PCIE GPP3

GPP3\_RX9P  
GPP3\_RX9N  
GPP3\_RX8P  
GPP3\_RX8N  
GPP3\_RX7P  
GPP3\_RX7N  
GPP3\_RX6P  
GPP3\_RX6N  
GPP3\_RX5P  
GPP3\_RX5N  
GPP3\_RX4P  
GPP3\_RX4N  
GPP3\_RX3P  
GPP3\_RX3N  
GPP3\_RX2P  
GPP3\_RX2N  
GPP3\_RX1P  
GPP3\_RX1N  
GPP3\_RX0P  
GPP3\_RX0N

AH10  
AG10  
AG11  
AE11  
AH12  
AG12  
AG13  
AE13  
AH14  
AG14  
AG15  
AE15  
AH16  
AG16  
AG17  
AE17  
AH18  
AG18  
AG19  
AE19

PCI\_E slot TX need CAP close to slot side

(19) PCIE5\_IP ML\_IP (33) ML\_IN  
(19) PCIE2\_IP PCIE2\_IN (19) PCIE1\_IP PCIE1\_IN (19) PCIE1\_IP PCIE1\_IN (31) USB3\_IP USB3\_IN (31) USB3\_IN  
AC21 SB\_RX3P  
AD21 SB\_RX3N  
AE22 SB\_RX2P  
AF25 SB\_RX2N  
AG25 SB\_RX1P  
AG26 SB\_RX1N  
AH26 SB\_RX0P  
AH26 SB\_RX0N

PCIE ALINK

SB\_TX3P  
SB\_TX3N  
SB\_TX2P  
SB\_TX2N  
SB\_TX1P  
SB\_TX1N  
SB\_TX0P  
SB\_TX0N

AG22 A\_TX3P C NC11 0.1u4/X7R/16V/K A\_TX3P (14)  
AH22 A\_TX3N C NC12 0.1u4/X7R/16V/K A\_TX3N (14)  
AE21 A\_TX2P C NC14 0.1u4/X7R/16V/K A\_TX2P (14)  
AG21 A\_TX2N C NC13 0.1u4/X7R/16V/K A\_TX2N (14)  
AF23 A\_TX1P C NC15 0.1u4/X7R/16V/K A\_TX1P (14)  
AG23 A\_TX1N C NC16 0.1u4/X7R/16V/K A\_TX1N (14)  
AG24 A\_TX0P C NC18 0.1u4/X7R/16V/K A\_TX0P (14)  
AH24 A\_TX0N C NC17 0.1u4/X7R/16V/K A\_TX0N (14)

PLACE THESE CAP CLOSE TO NB.

EXP A\_TXP[0..15] &gt;&gt; EXP\_A\_TXP[0..15] (18)

EXP A\_TXN[0..15] &gt;&gt; EXP\_A\_TXN[0..15] (18)

EXP A\_RXP[0..15] &gt;&gt; EXP\_A\_RXP[0..15] (18)

EXP A\_RXN[0..15] &gt;&gt; EXP\_A\_RXN[0..15] (18)

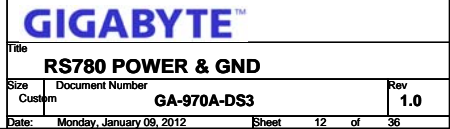
NB\_VCC  
NR2 1.27K/4/1 AE20  
NR3 1.82K/4/1 AD20  
NR4 1.27K/4/1 AE10  
NR5 1.82K/4/1 AD10  
NR6 1.27K/4/1 F14  
NR7 1.82K/4/1 E14

RX980/BGA692

GIGABYTE™

Title  
RS780 PCIE I/F ,SwitchSize Custom Document Number  
GA-970A-DS3Rev  
1.0

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## NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

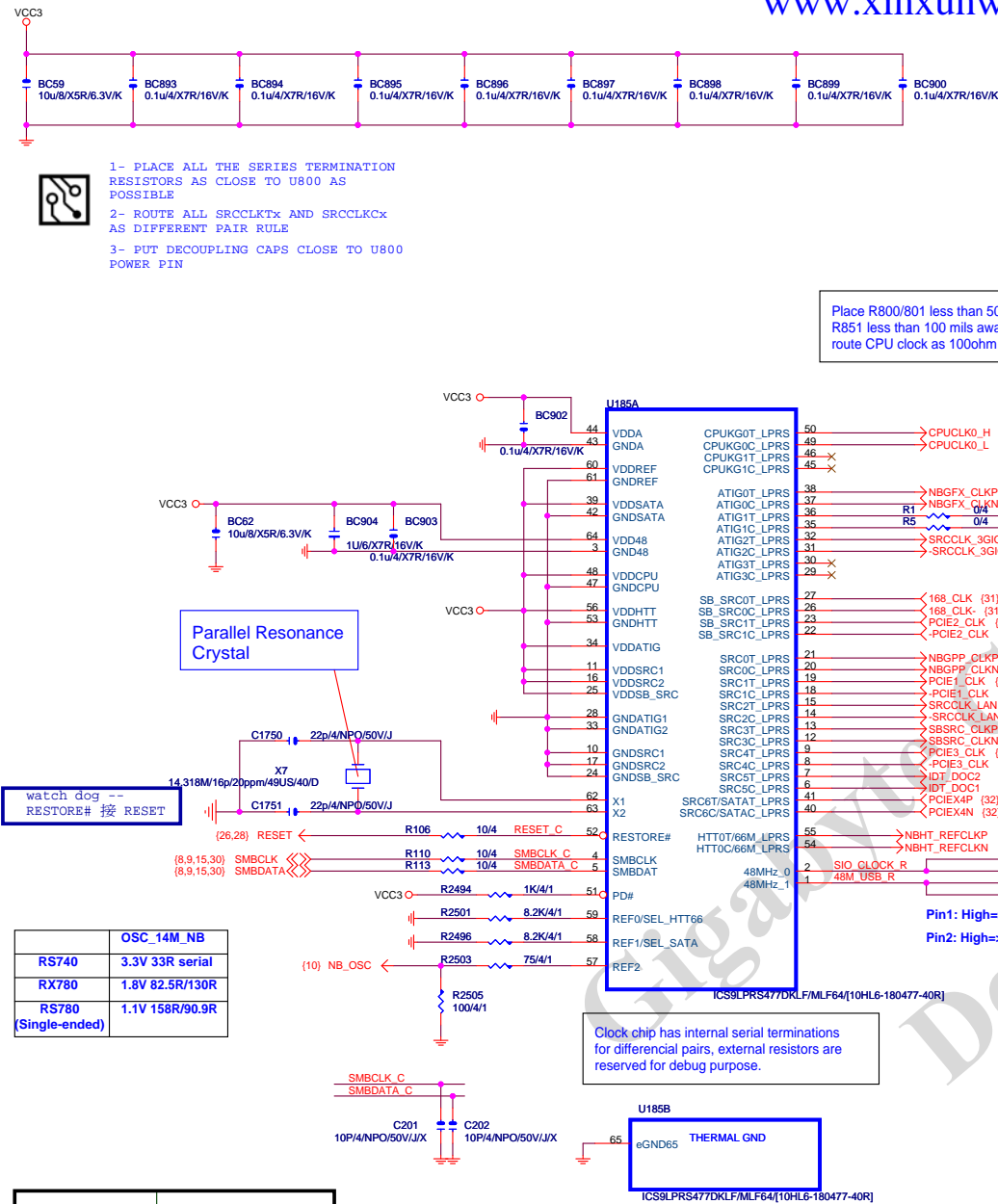
\* the GFX\_REFCLK input is required for all cases

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE

2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN

Place R800/801 less than 500 mills away from U800  
R851 less than 100 mills away from R800/801  
route CPU clock as 100ohm differential pair



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

GIGABYTE™			
Title			
RTM880N-793			
Size	Document Number	Rev	
Custom	GA-970A-DS3	1.0	
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**S.B HEATSINK**



NOT ADD ICT FOR RTCVDD PIN

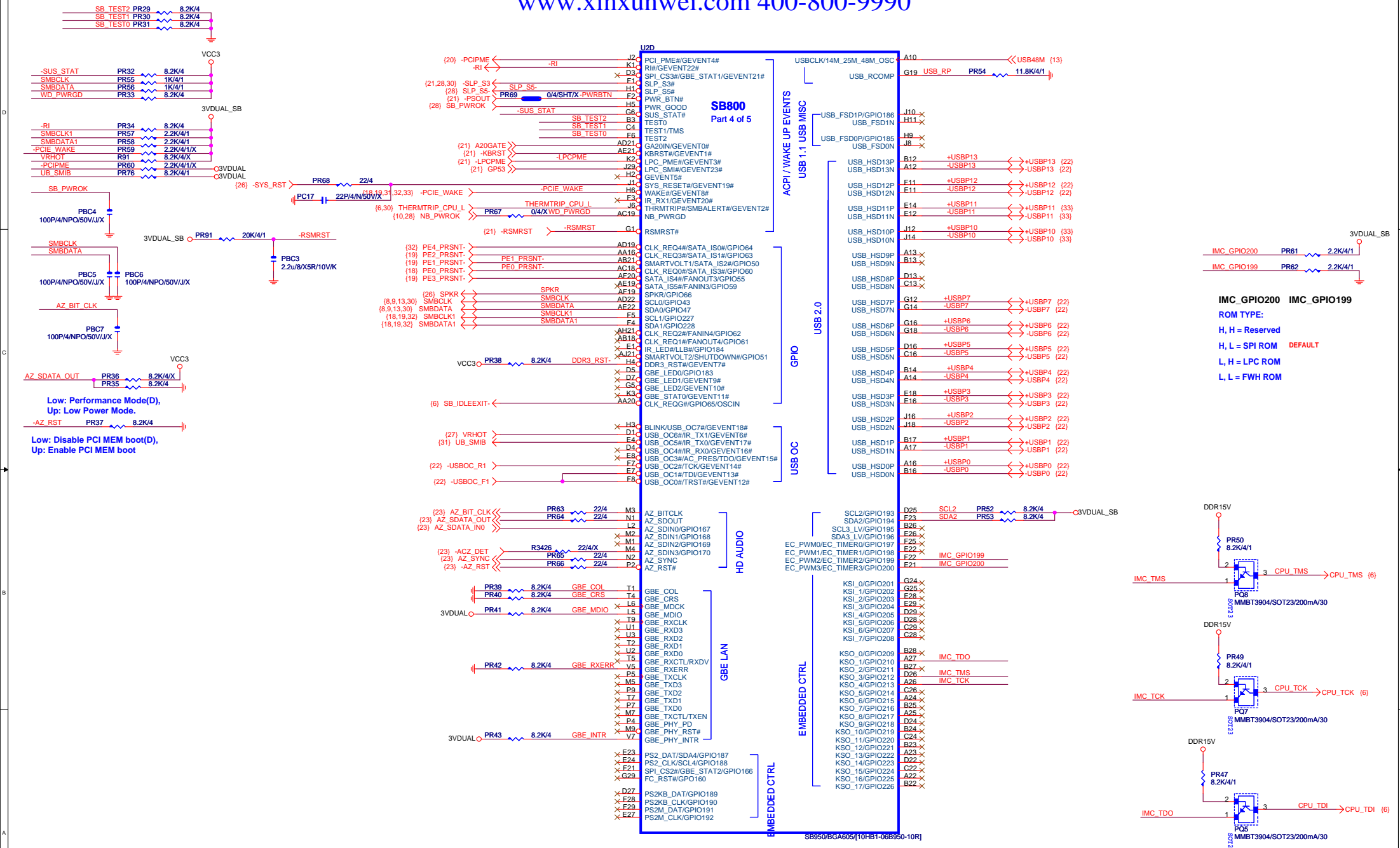
**GIGABYTE™**

Title	ATI SB700 PCIE/PCI/CPU/LPC
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Size	Document Number	Rev
Custom	<b>GA-970A-DS3</b>	<b>1.0</b>

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PLACE SATA\_CAL  
RES VERY CLOSE  
TO BALL OF U600

# NOTE:

R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK

VCC\_SB 1K/4/1 PR75 931/4/1 PR74

(26) -SATA\_LED -SATA\_LED AD11

TP5 -SATA\_X1 AD16

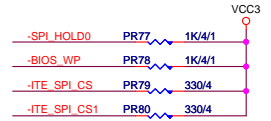
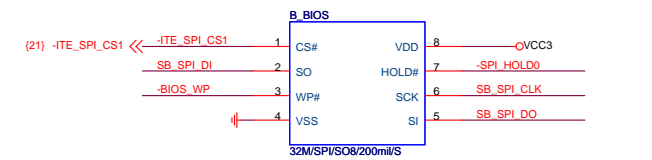
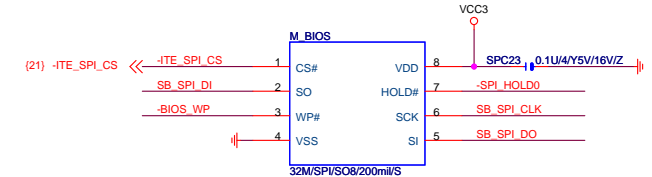
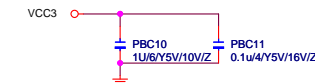
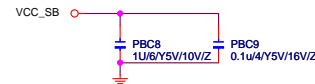
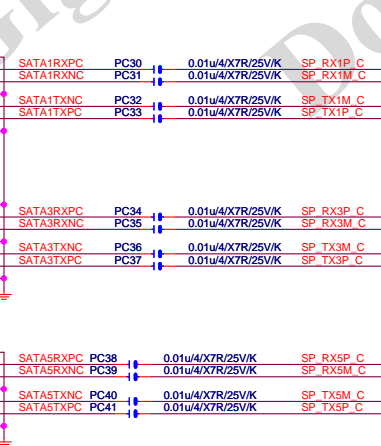
TP7 -SATA\_X2 AC16

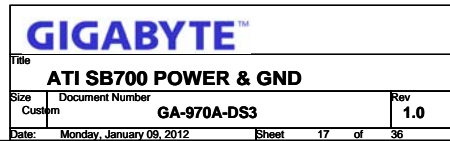
SB SPI DI PR70 22/4 SB SPI DI R J5  
SB SPI DO PR71 22/4 SB SPI DO R F2  
SB SPI CLK PR72 22/4 SB SPI CLK R K4  
SB SPI CS\_ITE PR73 22/4 SB SPI CS\_ K9  
X G2C

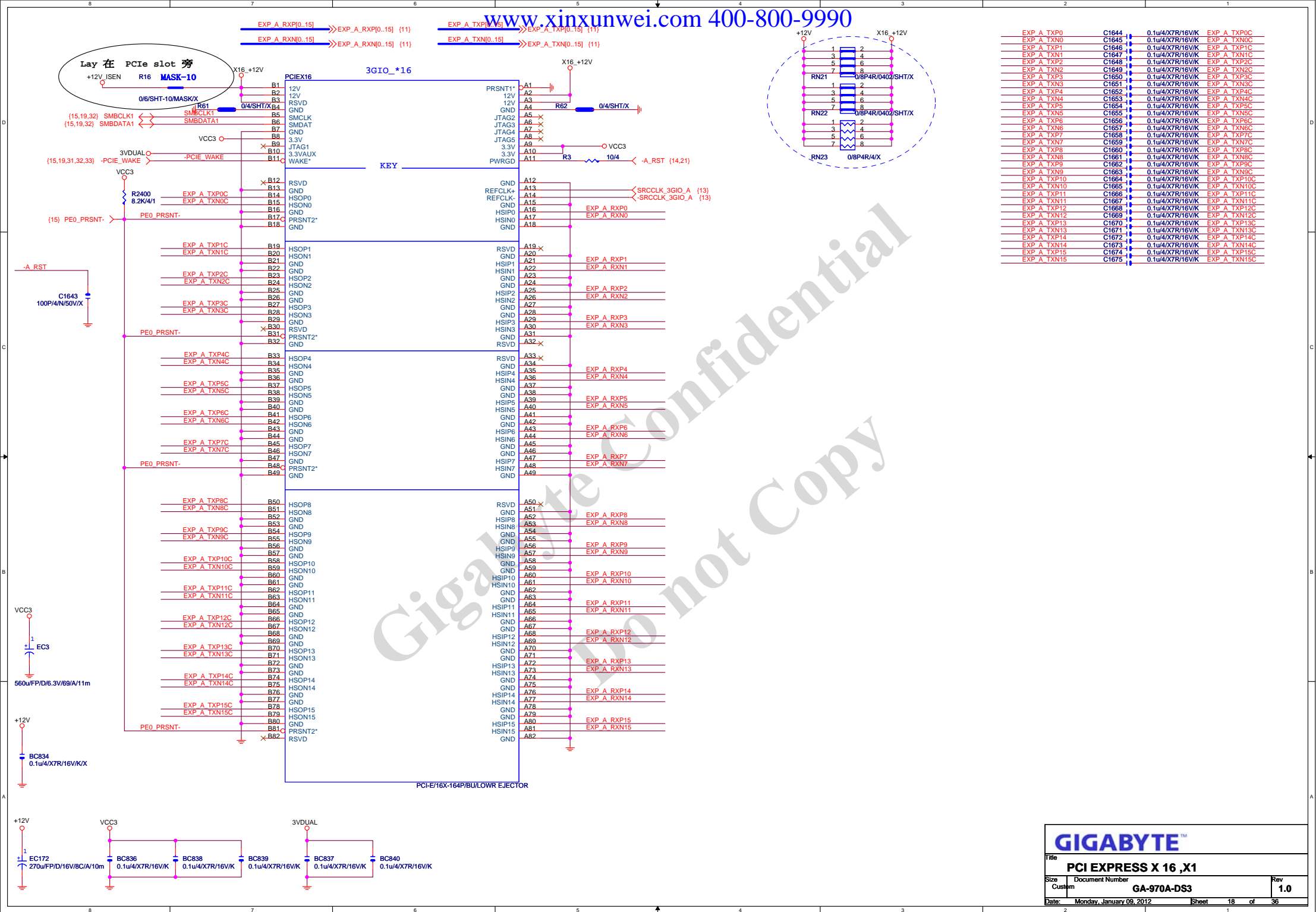
SB950/BGA805(10HB1-06B950-10R)

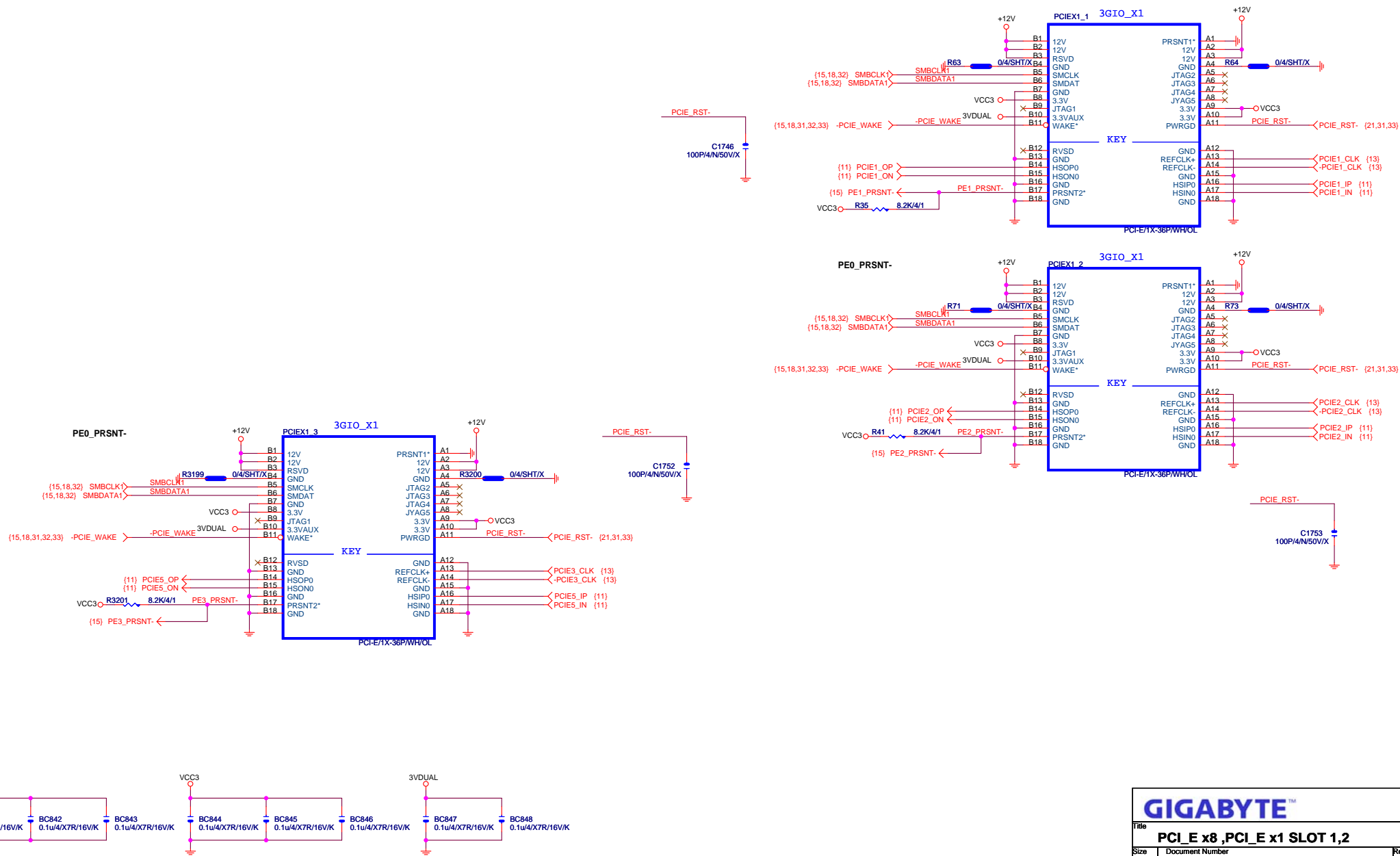


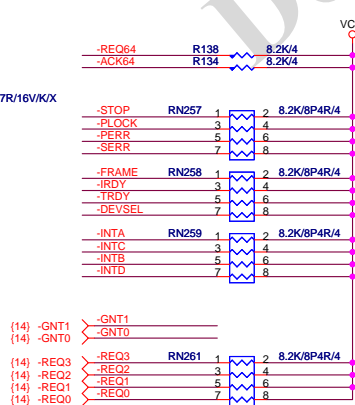
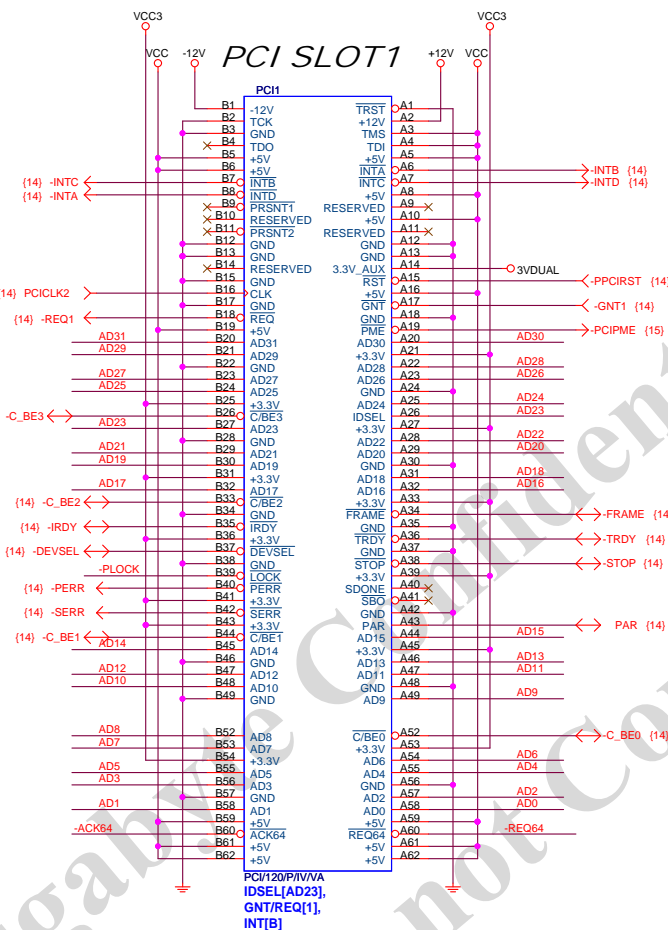
PLACE SATA AC COUPLING  
CAPS CLOSE TO SB850







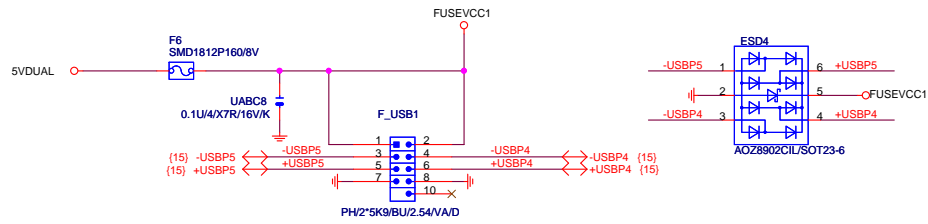




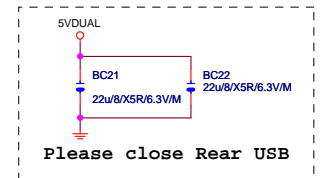
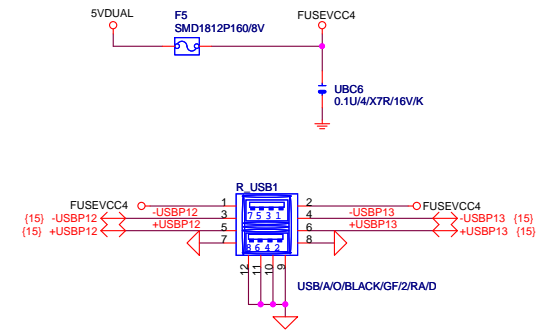




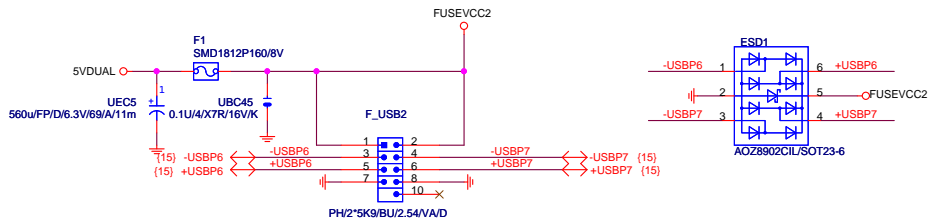
## FRONT SIDE USB1



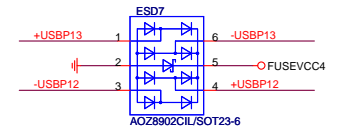
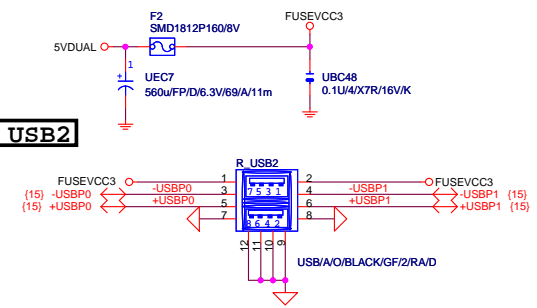
## REAR USB1



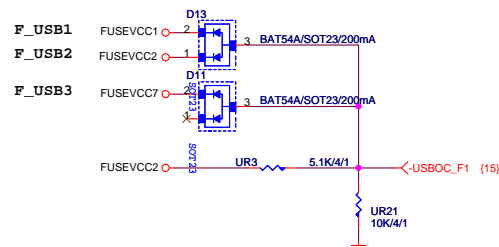
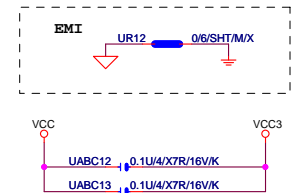
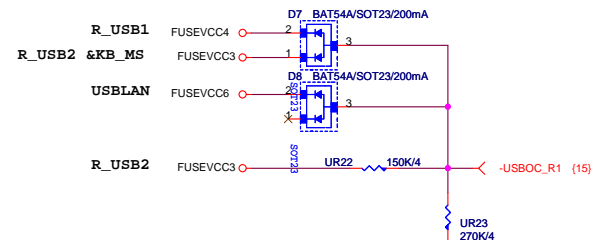
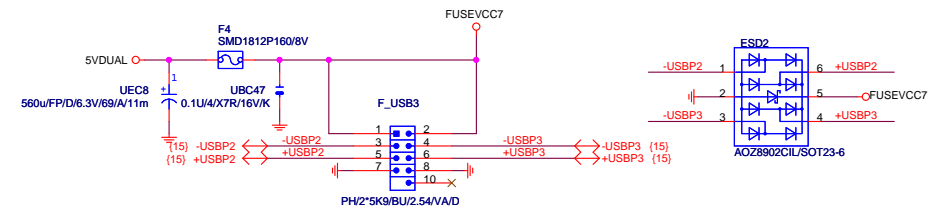
## FRONT SIDE USB2



## REAR USB2



## FRONT SIDE USB3

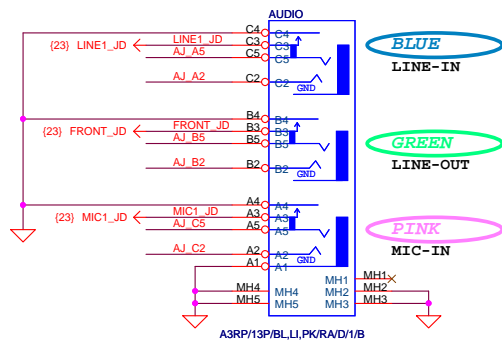
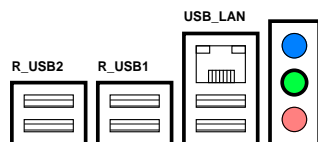
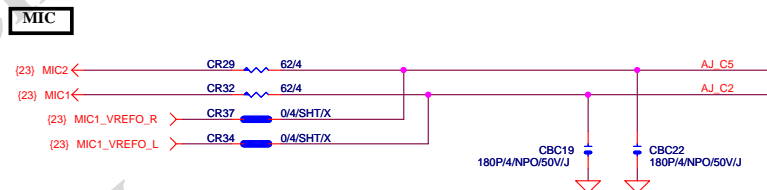
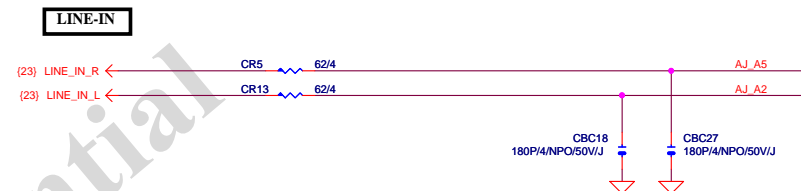
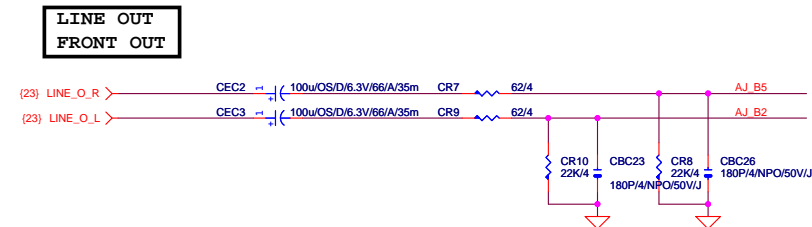
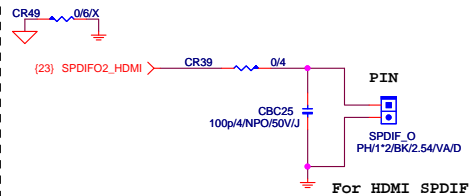




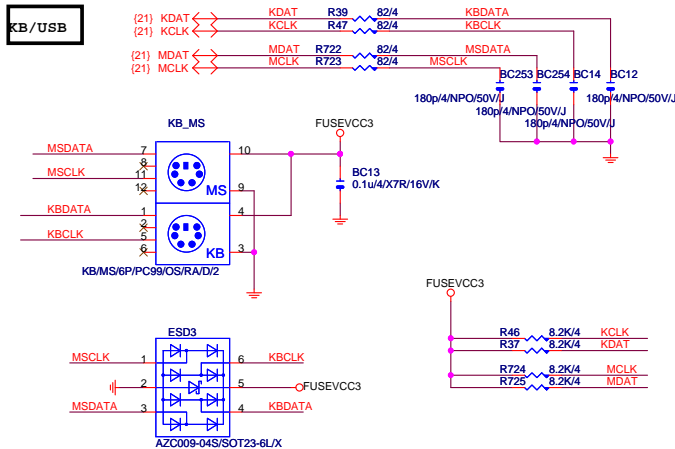
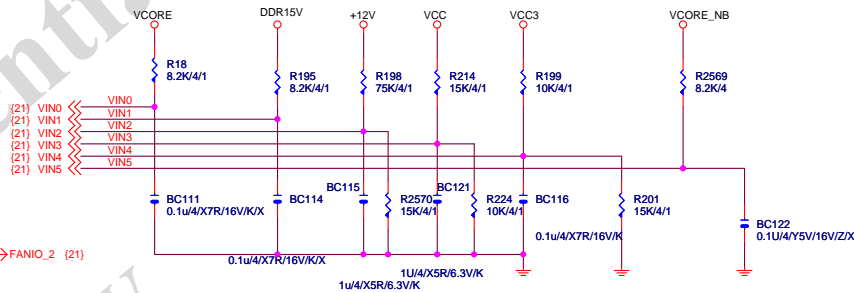
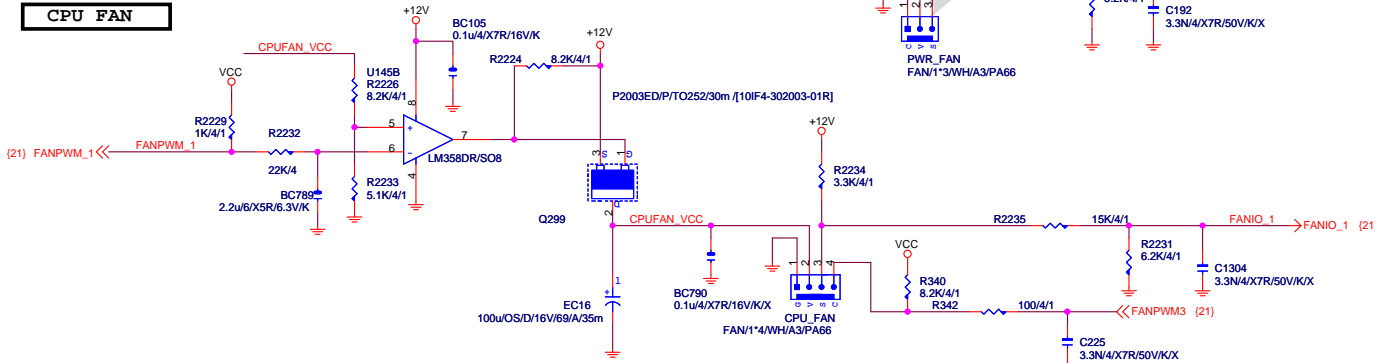
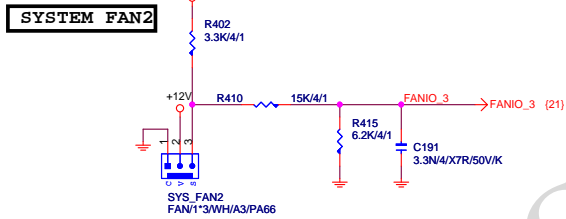
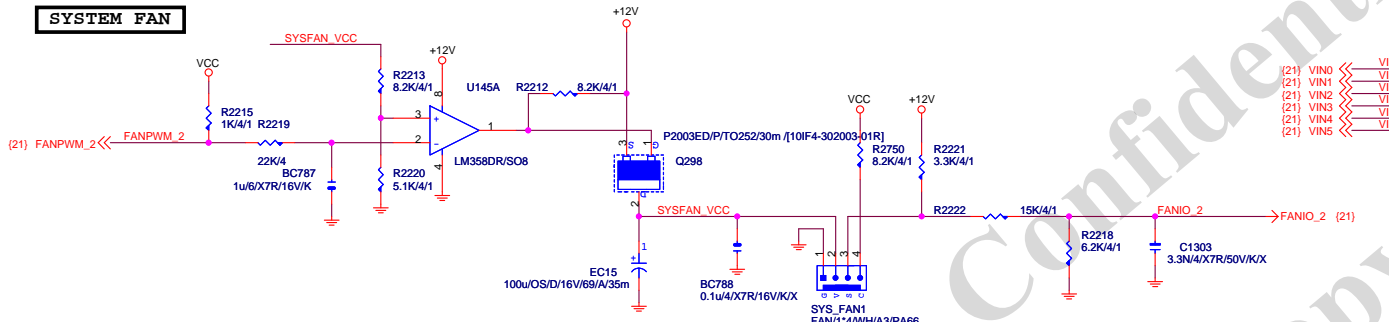
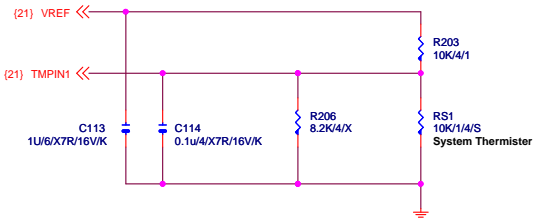


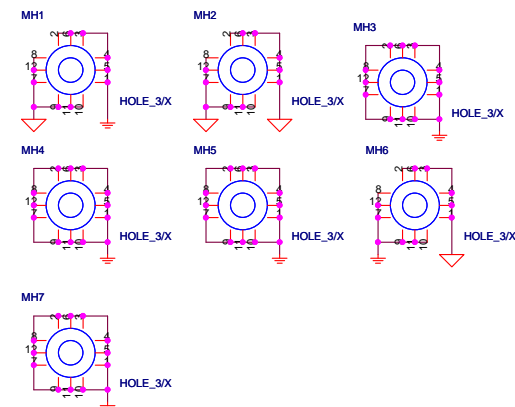
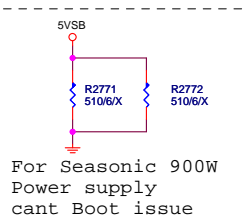
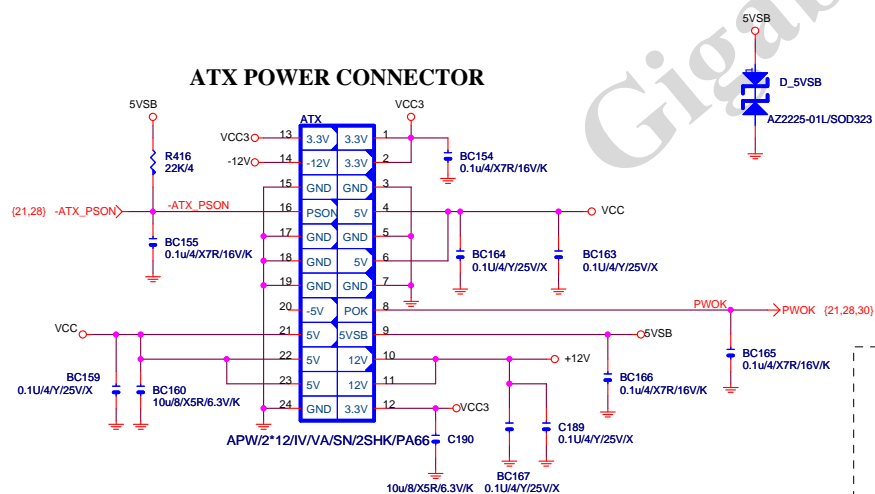
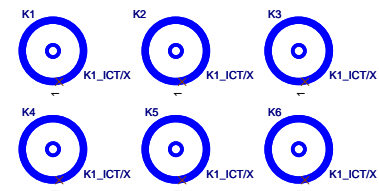
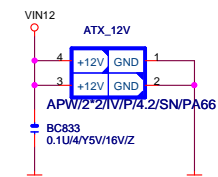
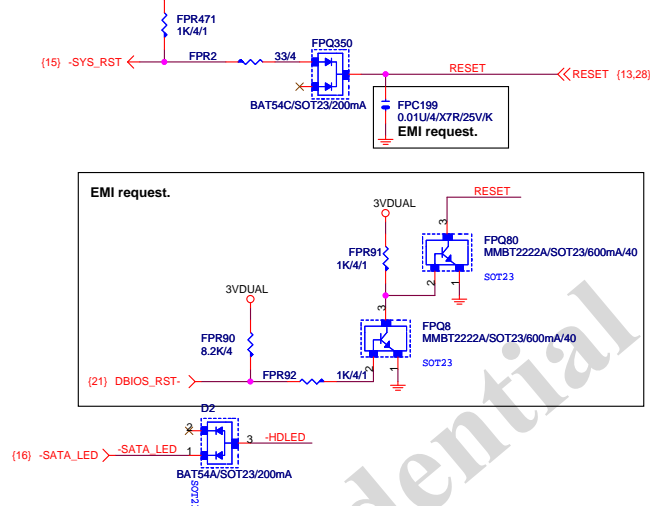
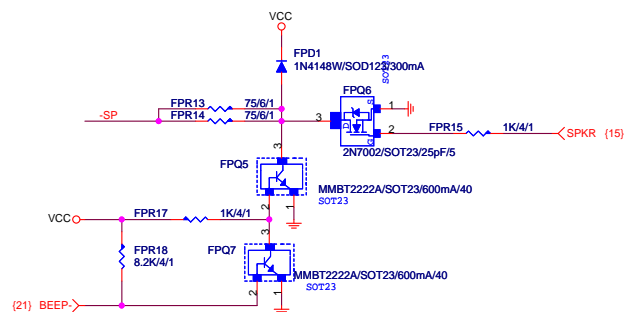
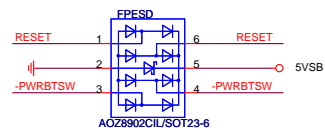
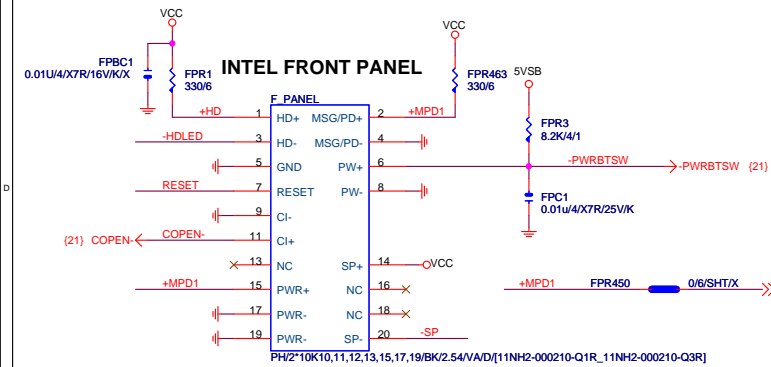


ADD CD2 For ESD PROTECT DIODE



Hardware Monitor circuits





www.xinxunwei.com 400-800-9990

RT8868

Disable PWM4 Use 3 Phase only

Disable PWM4 need pull high VCC5

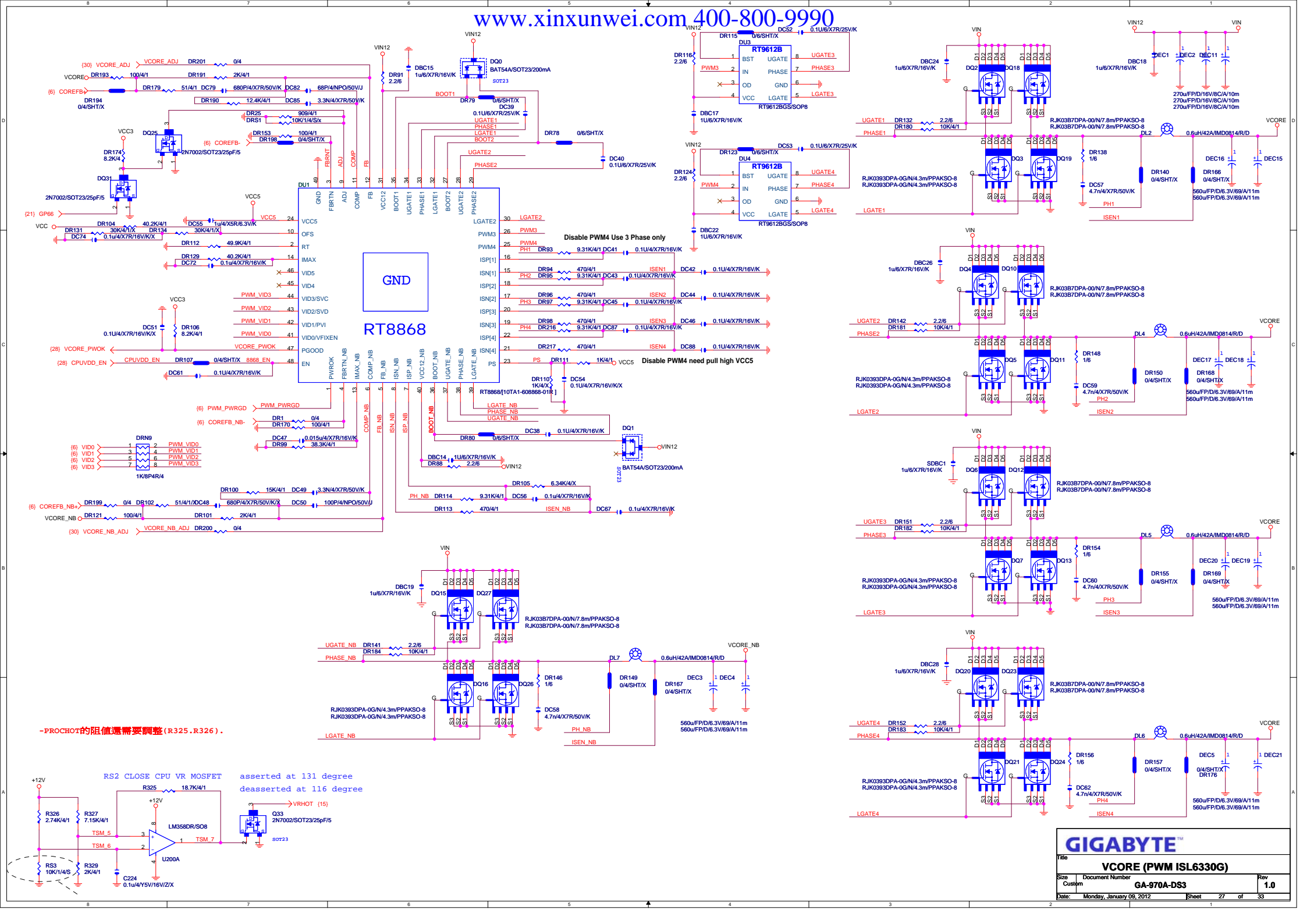
RS2 CLOSE CPU VR MOSFET asserted at 131 degree deasserted at 116 degree

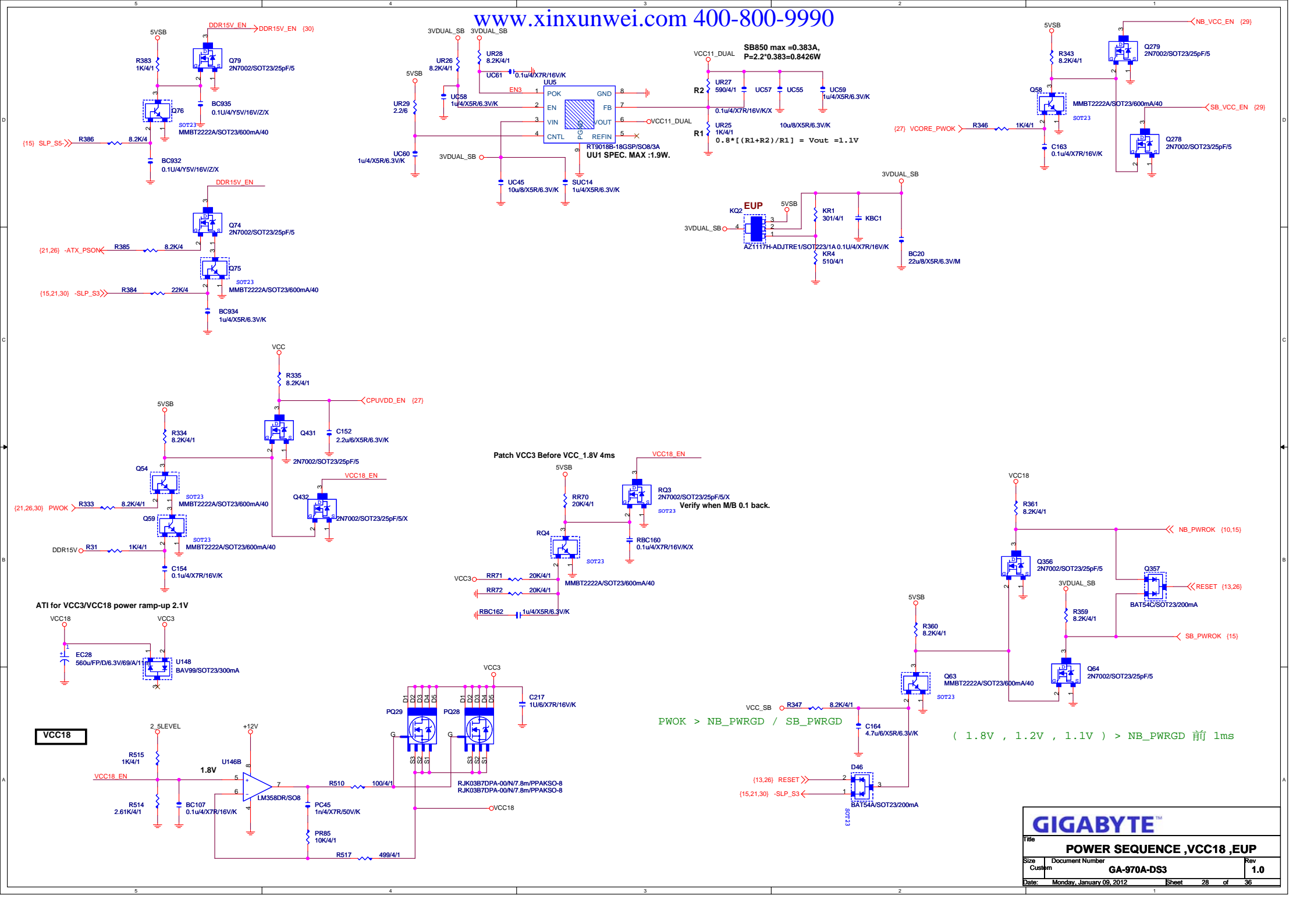
GIGABYTE

File: Vcore (PWM ISL6330G)

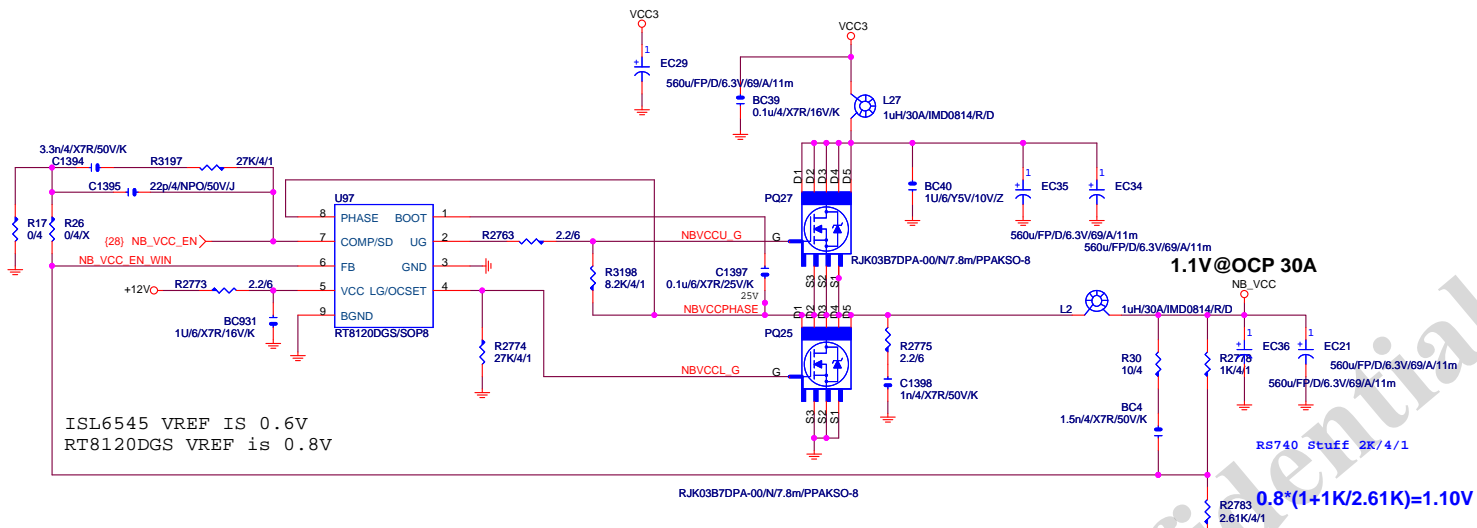
Size: Document Number GA-970A-DS3 Rev 1.0

Date: Monday, January 09, 2012 Sheet 27 of 33

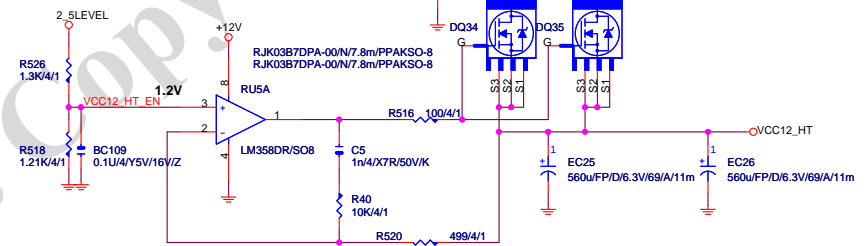




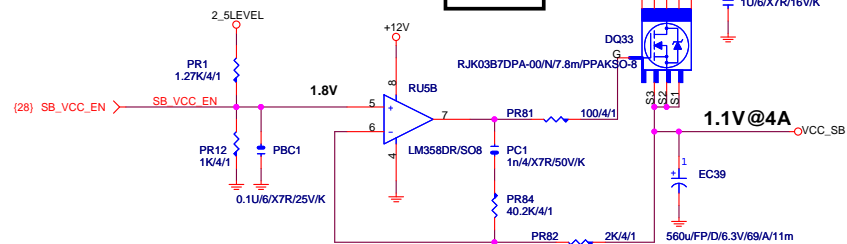
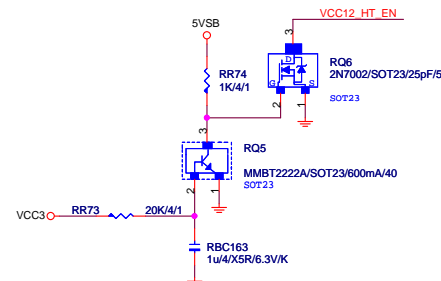
VCC\_NB



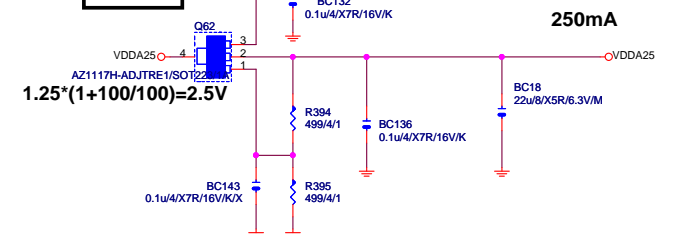
VCC12\_HT



VCC\_SB

Patch AMD Validation  
VDDA25 & VCC12\_HT  
power sequence

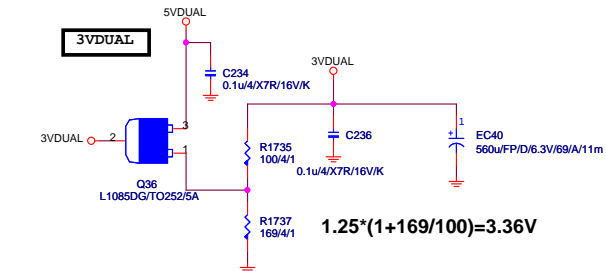
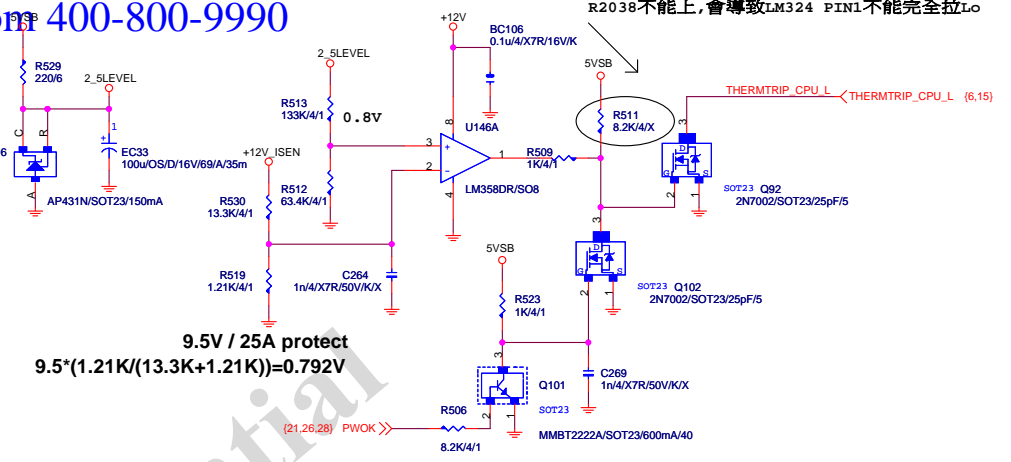
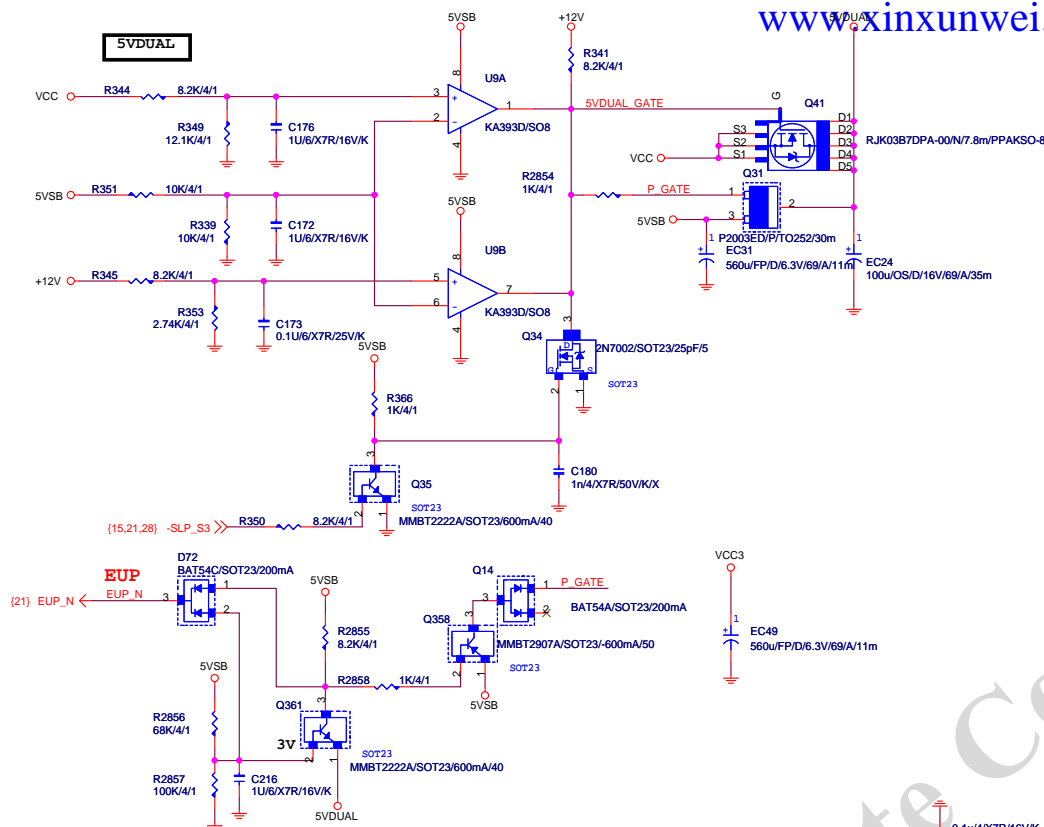
VDDA25



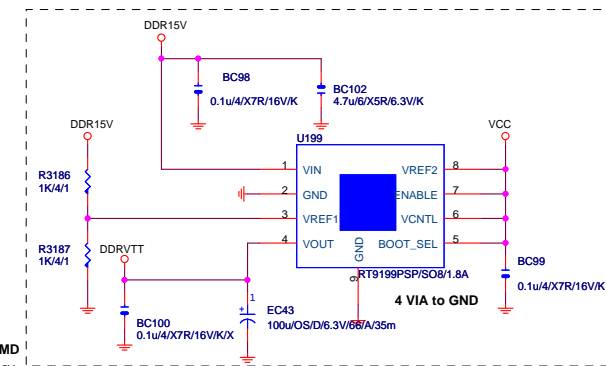
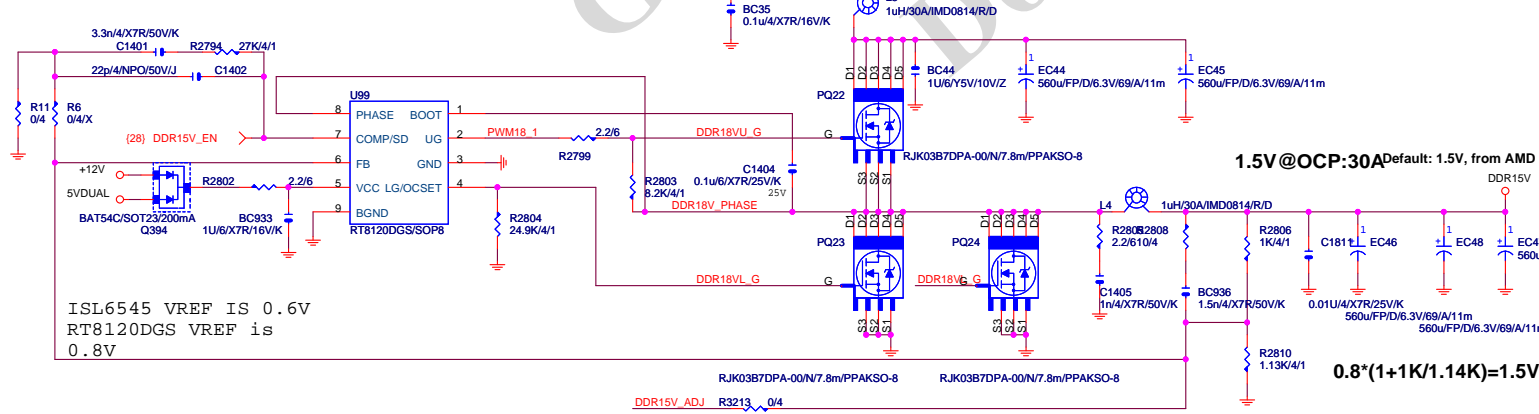
GIGABYTE

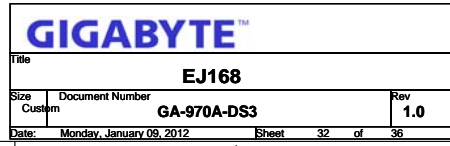
Title			GA-970A-DS3
Size			1.0
Date			Monday, January 09, 2012
Sheet			29 of 36





ISL6545 R9=>0, R8=>NC  
RT8120 R9=>NC, R8=>0

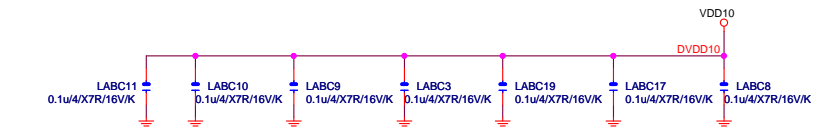
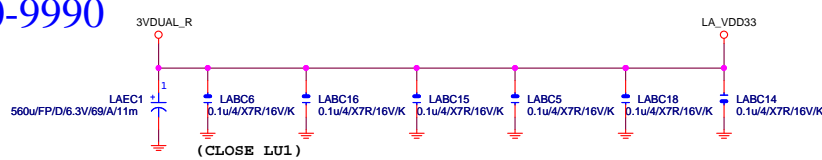
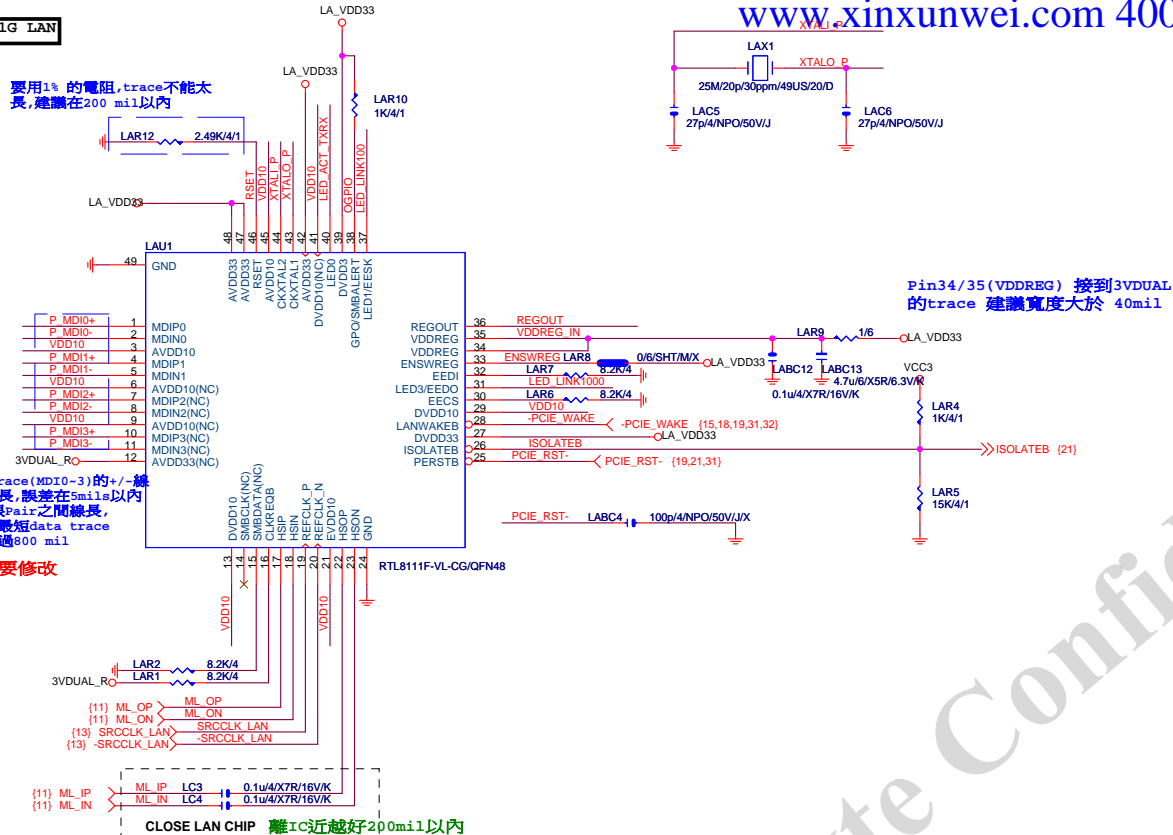




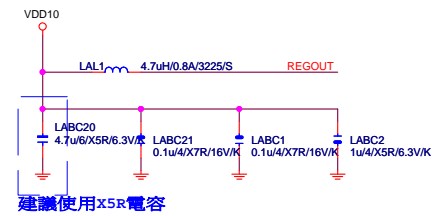
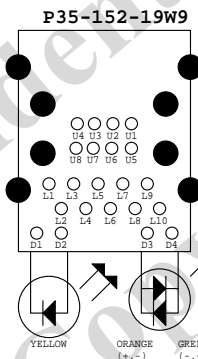


## PCIE-1G LAN

要用1% 的電阻,trace不能太長,建議在200 mil以內

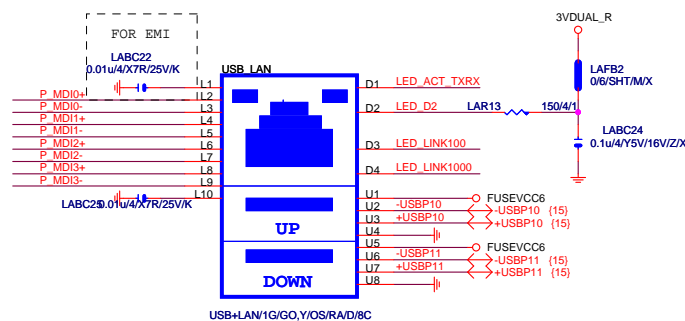
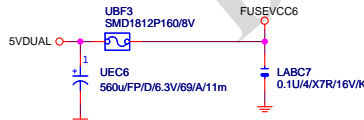
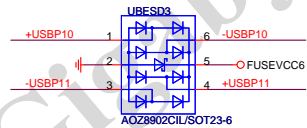


**USB\_LAN CONNECTOR**



USB\_LAN

```
RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8111C:LC6-->O
RTL8102E:LC5/LC6-->O
```



```

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS  DISABLE MDI-X FUNCTION)
-----
1G  :USB+LAN/1G/GO,Y/OS/RA/D/1      | EMI      LR1
100M:USB+LAN/100/GO,Y/OS/RA/D/1    |

```

